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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,947	08/31/2001	Brian P. Evans	0325.00504	2065

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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,947	EVANS ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 4, 6, 7, 8, 9, 10, 11, 20, 12, 19, 13, 14, 18, 15, 17, 16, are rejected under 35 U.S.C. 102(e) as being anticipated by Agrawal et al. (U.S. Patent No. 5015884).

Regarding claim 1, Agrawal et al. discloses the limitation of an apparatus comprising: a circuit comprising a distributed multiplexer configured to receive a distributed input group of signals, wherein said distributed multiplexer is configured to evenly load said distributed input groups (Figure. 2A, Abstract, lines 1 – 10; column 3, lines 4 – 13).

Regarding claim 4, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said circuit comprises a programmable interconnect matrix (PIM) (column 18, lines 41 – 42).

Regarding claim 6, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said circuit is configured to provide flexible reprogramming of said distributed multiplexer (column 13, lines 51 – 55).

Regarding claim 7, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said circuit is scalable (Abstract, lines 14 – 16; column 18, lines 6 – 8).

Regarding claim 8, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein a configuration of said circuit is expandable in a horizontal direction (column 18, lines 6 – 8; column 32, lines 15 – 30).

Regarding claim 9, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said configuration of said circuit is expandable in a vertical direction (column 18, lines 6 – 8; column 32, lines 31 – 37).

Regarding claim 10, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said configuration reduces complexity of physical routes of said distributed input groups (column 18, lines 8 – 16).

Regarding claims 11, 20, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein a layout or said circuit is deterministic (column 18, lines 6 – 18).

Regarding claims 12, 19, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein a delay of said circuit is deterministic (column 13, lines 23 – 25).

Regarding claim 13, Agrawal et al. discloses the limitation of an apparatus comprising: one or more input groups (Figure 9, column 14, lines 54 – 56); and one or more configurable matrices each configured to generate an output in response to said input groups, wherein said input groups are shared across said configurable matrices (column 14, lines 56 – 64).

Regarding claims 14, 18, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said input groups are constant across said configurable matrices (column 15, lines 50 – 60).

Regarding claims 15, 17, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein each of said configurable matrices comprise: one or more multiplexers configured to generate said output in response to said input groups (column 15, lines 61 – 67; column 16, lines 29 – 42).

Regarding claim 16, Agrawal et al. discloses the limitation of the apparatus according to claimed wherein said multiplexers comprise: two or more

bits configured to generate said output in response to said input groups (column 10, lines 39 – 50).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al. (U.S. Patent No. 5015884) in view of Graf (U.S. Patent No. 5869982).

Regarding claim 2, Agrawal et al. discloses the limitation of an apparatus comprising: a circuit comprising a distributed multiplexer configured to receive a distributed input group of signals, wherein said distributed multiplexer is configured to evenly load said distributed input groups (Figure. 2A, Abstract, lines 1 – 10; column 3, lines 4 – 13). Agrawal et al. does not disclose expressly the apparatus according to claimed wherein said distributed multiplexer comprise a plurality of bits each configured to evenly load said input groups. Graf discloses the limitation of the apparatus according to claimed wherein said distributed multiplexer comprise a plurality of bits each configured to evenly load said input groups (column 2, lines 1 – 3). It would have been obvious to modify Agrawal et

al. to include the apparatus according to claimed wherein said distributed multiplexer comprise a plurality of bits each configured to evenly load said input groups such as that taught by Graf in order to provide programmable logic devices having a data conversion capability.

Regarding claim 3, Agrawal et al. discloses the limitation of an apparatus comprising: a circuit comprising a distributed multiplexer configured to receive a distributed input group of signals, wherein said distributed multiplexer is configured to evenly load said distributed input groups (Figure. 2A, Abstract, lines 1 – 10; column 3, lines 4 – 13). Agrawal et al. does not disclose expressly the apparatus according to claimed wherein said bits of one distributed multiplexer are interleaved with at least another distributed multiplexer. Graf discloses the limitation of the apparatus according to claimed wherein said bits of one distributed multiplexer are interleaved with at least another distributed multiplexer (column 22, lines 45 – 50). It would have been obvious to modify Agrawal et al. to include the apparatus according to claimed wherein said bits of one distributed multiplexer are interleaved with at least another distributed multiplexer such as that taught by Graf in order to provide programmable logic devices having a data conversion capability.

Regarding claim 5, Agrawal et al. discloses the limitation of an apparatus comprising: a circuit comprising a distributed multiplexer configured to receive a distributed input group of signals, wherein said distributed multiplexer is configured to evenly load said distributed input groups (Figure. 2A, Abstract, lines

1 – 10; column 3, lines 4 – 13). Agrawal et al. does not disclose expressly the limitation of the apparatus according to claimed wherein said bits comprise programmable interconnect matrix (PIM) bits. Graf discloses the limitation of the apparatus according to claimed wherein said bits comprise programmable interconnect matrix (PIM) bits. (Fig. 6, column 2, lines 1 – 3; column 22, lines 45 – 50). It would have been obvious to modify Agrawal et al. to include the apparatus according to claimed wherein said bits comprise programmable interconnect matrix (PIM) bits such as that taught by Graf in order to provide programmable logic devices having a data conversion capability.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ajit Patel
Primary Examiner

ACL AU::2664 May 04, 2005